REMARKS

By this Amendment, Applicants add new claims 16-20.

Accordingly, claims 1-20 remain pending in the application.

Applicants thank the Examiner for acknowledging the claim for priority and receipt of certified copies of the priority document.

The Examiner is respectfully requested to state whether the drawings are acceptable.

Reexamination and reconsideration are respectfully requested.

35 U.S.C. § 102

The Office Action rejects claims 1-3 under 35 U.S.C. § 102 over <u>Blanchard</u> U.S. Patent 6,331,794 ("<u>Blanchard</u>"). Applicants respectfully traverse those rejections for at least the following reasons.

Claim 1

The array of claim 1 includes N DMOS transistors laterally arranged in a epitaxial layer, wherein the N DMOS transistors share in common either a source or a drain.

M.P.E.P. § 2131 provides that:

"TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM 'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.'

Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)"

(emphasis in original).

Here, Applicants respectfully submit that <u>Blanchard</u> does not disclose N DMOS transistors laterally arranged in a epitaxial layer, nor does he disclose N DMOS transistors sharing either a source or a drain.

Blanchard FIG. 1, the only figure which shows any epitaxial layer, shows only one DMOS transistor. Nothing in Blanchard discloses - either expressly or inherently - that any other DMOS transistors are or should be laterally arranged in a same epitaxial layer.

Nor does <u>Blanchard</u> FIG. 1 disclose that N DMOS transistors share a source or drain.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over <u>Blanchard</u>.

Claims 2-3

Claims 2-3 depend from claim 1 and are therefore deemed patentable over Blanchard for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 3

In claim 3, the DMOS transistors are lateral DMOS transistors sharing either a common source or drain.

Applicants respectfully submit that no such feature is either disclosed or even suggested by <u>Blanchard</u>.

The Office Action notes that <u>Blanchard</u> states in col. 1 that a MOSFET can be a lateral structure. However, <u>Blanchard</u> does not state that a DMOS transistor, in particular, can have a lateral structure and it does disclose that any array of such transistors should (or even <u>can</u>) share either a common source or drain. Furthermore, <u>Blanchard</u> certainly does not provide any enabling teaching to one of ordinary skill in the art as to how one would even construct any lateral DMOS array sharing either a common source or drain.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 3 is patentable over <u>Blanchard</u>.

NEW CLAIMS 16-20

New claims 16-20 all depend from claim 1 and are deemed patentable for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 16

Among other things, in the array of claim 16, one of the source or drain commonly shared among the N DMOS transistors surrounds the one of the source or drain of each double diffused MOS transistor formed unique to each DMOS transistor.

Applicants respectfully submit that no such feature is disclosed by <u>Blanchard</u>.

Claim 17

Among other things, in the array of claim 17, the common electrode for all of the DMOS transistors, and the unique electrodes for each of the DMOS transistors, are all disposed on a same side of the semiconductor substrate as each other.

Applicants respectfully submit that no such feature is disclosed by <u>Blanchard</u>. <u>Claim 18</u>

Among other things, in the array of claim 18, one of the source or drain commonly shared among the N DMOS transistors surrounds the one of the source or drain of each double diffused MOS transistor formed unique to each DMOS transistor.

Applicants respectfully submit that no such feature is disclosed by Blanchard.

Claim 19

Among other things, in the array of claim 19, the epitaxial layer is of a first conductivity type and the source and drain are of a second conductivity type different from the first conductivity type.

Applicants respectfully submit that no such feature is disclosed by <u>Blanchard</u>. <u>Claim 20</u>

Among other things, the array of claim 20 includes a buried layer interposed between the substrate and the epitaxial layer, where the epitaxial layer and the buried layer each have a first conductivity type, and where the buried layer is more heavily doped than the epitaxial layer.

Applicants respectfully submit that no such feature is disclosed by Blanchard.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-20, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (703) 715-0870 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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